

## **XE3000™ Load Test Results**

**Date:** 27 February 2012

**Hardware:**

CPU: Intel i3-2120 (3.3 GHz, 2 cores)

RAM: 4 GB, DDR3 1333 MHz

Motherboard: Intel S1200KP

**Software Version:**

Elastix: 2.2

DAHDI: 2.5.0.2.svn.r10467-1 (compiled without MMX optimization)

Asterisk: 1.8.9.1

**Test Conditions:**

1. The Hyper Threading was disabled in the BIOS settings.
2. Astribank drivers were compiled with an enabled OPTIMIZE\_CHANMUTE parameter. As a result, Astribank drivers do not send voice packets for DAHDI performance (echo cancellation, etc.) for channels with no active calls. This option is applied for FXS/FXO channels. The E1/T1 channels are not affected.
3. Asterisk was running without the real time priority.
4. All FXS extensions were configured for immediate start. The Asterisk extensions context was defined as follows:

```
[music-test]
exten => s,1,Answer()
exten => s,2,Playback(music-8khz-10min)
exten => s,3,Goto(2)
```

The calls were initiated by analog telephone simulators.

1. Used G.729 codec: Open source codec\_g729-ast18-gcc4-glibc-pentium4.so
2. To be included in the number of maximum simultaneous calls, the voice in the call had to be clear, without interruptions.

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**Test #1: XE3000/XR3000 with 8 XR0008 devices (32 FXS ports each) connected.**

FXS extensions: 256  
 IO ports 48  
 Total number of DAHDI channels: 304

Echo Cancellor Tail Size (taps <sup>ii</sup> )	Maximum Number of Calls		
	i3-2120 (XE3000 H/W rev. 3.0)	E8400 (XR3000)	Q9550 (XE3000 H/W rev. 2.0)
256	80	72	71
128	152	Not tested	Not tested

**Test #2: XE3000/XR3000 with an XR0056 device (4 E1/T1 ports) connected and G.729 SIP calls and call recording enabled.**

E1 ports: 4  
 Total number of DAHDI channels: 120

Echo Cancellor Tail Size (taps)	Maximum Number of Calls	
	i3-2120 (XE3000 H/W rev. 3.0)	Q9550 (XE3000 H/W rev. 2.0)
256	110	93

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<sup>ii</sup> "Taps": The echo cancelling algorithm operates by generating multiple copies of the received signal, each delayed by some small time increment. In digital terms, this is the equivalent of a shift register and each delayed signal appears at its own unique "tap". The number of taps determines the size of the echo delay that can be cancelled. These delayed copies are then scaled (or weighted) and subtracted from the original received signal. (source: Wikipedia)

